## ABSTRACT OF THE DISCLOSURE

Flip-flop circuit arrangement

A flip-flop circuit arrangement having a total of four differential amplifiers (1, 2, 3, 4), which are connected to one another to produce a D flip-flop, is specified. According to the suggested principle, the two shared emitter nodes (E1, E2) of the differential amplifiers (1, 2, 3, 4) are connected via a switch pair (S1, S2) to supply potential and are activated by a differential input clock signal at a control input (CN, CP). The present flip-flop circuit is operable using especially low supply voltage (VCC) and is preferably suitable for constructing frequency dividers or shift registers.

Figure